Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method, comprising:

providing at least three elements, including a first element and a last element, each element having an associated parameter;

providing a first identifier for the first element;

for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;

saving the transform; and

for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element.

2-6 (Cancelled)

7. (Original) The method of claim 1, wherein performing the second operation includes:

shifting the first identifier to produce a shifted identifier; and

performing an exclusive OR operation on the shifted identifier and the transform to produce the last identifier.

8. (Cancelled)

9. (Original) The method of claim 1, wherein the at least three elements are branch instructions in an instruction execution pipeline.

10. (Currently Amended) The method of claim 1, further comprising:

using ~~the~~ a last index to access a location in a prediction array; and

using a content of said location to predict a decision status of the last element.

11-20 (Cancelled)

21. (Original) A circuit, comprising:

a register;

a data shifting circuit having an input coupled to an output of the register;

an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;

an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit; and

a prediction logic circuit coupled to an output of the exclusive OR circuit.

22. (Cancelled)

23. (Original) The circuit of claim 21, wherein the data shifting circuit includes a plurality of inputs coupled to the output of the register to shift data from the register by a selected number of bits.

24. (Original) A computer system comprising:

an instruction execution pipeline;

a transform generation circuit coupled to the instruction execution pipeline and including:

a register;

a data shifting circuit having an input coupled to an output of the register;

an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;

an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit; and

a prediction logic circuit coupled to an output of the exclusive OR circuit.

25. (Cancelled)

26. (Original) The computer system of claim 24, wherein the data shifting circuit includes a plurality of inputs coupled to the output of the register to shift data from the register by a selected number of bits.

27. (Original) A machine-readable medium having stored thereon instructions, which when executed by at least one processor cause said at least one processor to perform:

providing at least three elements, including a first element and a last element, each element having an associated parameter;

providing a first identifier for the first element;

for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;

saving the transform;

for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element;

using the last identifier to access a location in a prediction array; and

using a content of said location to predict a decision status of the last element.

COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on May 18, 2004. At the time the Examiner mailed the Office Action claims 1, 7, 9, 10, 21, 23, 24, 26, and 27 were pending. By way of the present response the Applicants have: 1) added no claims; 2) amended claim 10; and 3) cancelled no claims. As such, claims 1, 7, 9, 10, 21, 23, 24, 26, and 27 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims.

Specification Objections

The Examiner has objected to the Abstract of the Specification for containing over 150 words. Applicants have amended the Abstract to fit within the 150-word guideline and respectfully request the examiner to withdraw the objection.

Double Patenting

Claims 1, 9, 10, 21, 23, 24, 26 and 27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 6, 7, 19, 20, 21, 22 and 23, respectively of U.S. Patent No. 6,715,064. Applicants have concurrently filed a terminal disclaimer to overcome this rejection.

Claim Rejections

35 U.S.C. 112 Rejections

The Examiner rejected claim 10 under 35 U.S.C. 112 as claim 10 recited the limitation "the last index" in line 2, stating that there is insufficient antecedent basis for this limitation in the claim. Applicants have amended claim 10 to overcome this objection.

35 U.S.C. 102(e) Rejections

The Examiner rejected claims 21, 23, 24, and 26 under 35 U.S.C. 102(e) as being anticipated by Talcott, U.S. Patent 6,272,623 (hereinafter Talcott), cited in the IDS filed on October 20, 2003.

Claim 21 sets forth:

> A circuit, comprising:
> a register;
> a data shifting circuit having an input coupled to an output of the register;
> an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;
> an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit; and
> a prediction logic circuit coupled to an output of the exclusive OR circuit.

(emphasis added)

Therefore, claim 21 includes "an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit."

In regards to independent claim 21, the Examiner states the phrase "an array...further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit" is met by Talcott. Pg. 4, item 13 of the office action mailed 5/18/04. The Examiner states that the INSTRUCTION ADDRESS from Fig. 2 anticipates the above language of claim 21. Applicants' respectfully disagree. Fig. 2 of Talcott shows that an INSTRUCTION ADDRESS is coupled to Local History Table 220. To this end, Talcott states, "Each register stores the 1 most recent conditional outcomes for a set of instruction addresses that each have the same a address bits in common. When an instruction in this set results in a branch being taken, a value of 1 is shifted into the corresponding register. In contrast, a value of 0 is shifted into the corresponding register if a branch is not taken." Talcott, col. 3, lines 35-43. Emphasis added. This language does not disclose that an array is transferring data shift information to a data shifting circuit as claimed in claim 21. Instead, this language states that a value of 0 or 1 is shifted into a register based on whether or not a branch is taken. Nothing in Talcott is disclosing that an array is transferring such data shift information to a data shifting circuit. As such, Applicants respectfully submit that independent claim 21 and all its dependent claims are not anticipated by Talcott, and should be allowed as presented.

Independent claim 24 contains substantially the same limitations as claim 21 and is not anticipated by Talcott for the same reasons as mentioned above. As such, Applicants respectfully submit that independent claim 24 and all its dependent claims are not anticipated by Talcott, and should be allowed as presented.

35 U.S.C. 102(b) Rejections

The Examiner rejected claims 1, 9, 10 and 27 under 35 U.S.C. 102(b) as being anticipated by Pan, et al., U.S. Patent 5,553,253 (hereinafter Pan) cited in the IDS filed on October 20, 2003.

Claim 1 sets forth:

> A method, comprising:
> providing at least three elements, including a first element and a last element, each element having an associated parameter;
> providing a first identifier for the first element;
> for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;
> saving the transform; and
> for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element.

(emphasis added)

Therefore, claim 1 includes "providing at least three elements, including a first element and a last element, each element having an associated parameter."

In regards to claim 1, the Examiner states the phrase "providing at least three elements, including a first element and a last element, each element having an associated parameter" is met by Pan. Pg. 6, item 19 of the office action mailed 5/18/04. Applicants respectfully disagree. The Examiner refers to Figure 3, A27, A28 and A29 of Pan as being a parameter associated with the first element, or branch instruction. This may show that the first element is associated with a parameter (A27, A28 and A29), but it does not disclose that all three elements have an associated parameter. Fig. 3 of Pan shows that item 17 is a single branch

instruction. This is the only branch instruction disclosed. Hence there is no disclosure of three separate elements in which all three are associated with a parameter. As such, Applicants respectfully submit that claim 1 and all its dependent claims are not anticipated by Pan, and should be allowed as presented.

Independent claim 27 contains substantially the same limitations as claim 1 and is not anticipated by Pan for the same reasons as mentioned above. As such, Applicants respectfully submit that independent claim 27 and all its dependent claims are not anticipated by Pan, and should be allowed as presented.

The Examiner also rejected claims 1, 9, 10 and 27 under 35 U.S.C. 102(b) as being anticipated by Applicant's own admitted prior art in the specification.

As stated above, claim 1 sets forth:

> A method, comprising:
> providing at least three elements, including a first element and a last element, each element having an associated parameter;
> providing a first identifier for the first element;
> for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;
> saving the transform; and
> for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element.

(emphasis added)

Therefore, claim 1 includes "for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to a transform."

In regards to claim 1, the Examiner states the phrase "for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to a transform" is met by Applicants' own specification (specifically Fig. 1-3). Pg. 7, item 24 of the office action mailed 5/18/04. Applicants respectfully disagree. Claim 1 discloses "performing a first operation on the first identifier and at least one of the parameters to produce a transform." The prior art of Fig. 2 discloses that an "exclusive OR (XOR) function is performed on the shifted index value and the associated parameter." Pg. 8, lines 9-10. Fig. 2 is disclosing that the XOR function is performed on the shifted index's associated value and not at least one of the parameters as taught by claim 1. "The associated parameter" and "at least one of the parameters" are not the same.

Further, Fig.2 teaches that the "index is shifted one bit to the left" before the XOR function is performed on it. Pg. 8, line 9. This left-shift is not taught or suggested in claim 1. As such, Applicants respectfully submit that claim 1 and all its dependent claims are not anticipated by its own specification, and should be allowed as presented.

Independent claim 27 contains substantially the same limitations as claim 1 and is not anticipated by its own specification for the same reasons as mentioned above. As such, Applicants respectfully submit that independent claim 27 and all its dependent claims are not anticipated by its own specification, and should be allowed as presented.

In light of the comments above, the Applicants respectfully request the allowance of all claims.

Comments

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Michael J. Mallie at (408) 720-8300.

Respectfully submitted,

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